

Notice of References Cited	Application/Control No.	Applicant(s)/Patent Under Reexamination	
	10/611,467	PARULKAR ET AL.	
Examiner	Art Unit	2113	Page 1 of 1
Elmira Mehrmanesh			

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
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FOREIGN PATENT DOCUMENTS

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	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Marc E. Levitt, Designing UltraSparc for Testability Design & Test of Computers, IEEE Volume 14, Issue 1, Jan.-March 1997 Page(s):10 - 17
	V	Parulkar, I. et al., A scalable, low cost design-for-test architecture for UltraSPARC/spl trade/ chip multi-processors Test Conference, 2002. Proceedings. International 007-10 Oct. 2002 Page(s):726 - 735
	W	
	X	

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